earnestly solicited.

Respectfully submitted,

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JHM/HYL:nj

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT

Please amend the abstract by rewriting same to read as follows.

--A sampling frequency conversion apparatus which easily controls the phase difference (time difference) between the input data and the output data in converting the sampling frequency, [and comprises] includes a storage [means] device 13 for continuously writing the input data or the data obtained by over-sampling the input data and for continuously reading out the data written maintaining a predetermined address difference relative to the [write] writable address, and an interpolation processing [means] unit 14 for interpolating the data read-out from the storage [means] device 13 to obtain data of which the sampling frequency is converted. In converting the sampling frequency, an address difference between a [write] writable address and a [read] readable address in the storage [means] device 13 is optimized, the address difference being optimized without limitation for a predetermined period of time from the start of supplying the input data and, then, being optimized by imposing a predetermined limitation after the passage of the predetermined period of time.--

IN THE CLAIMS

Please amend claims 1-11 by rewriting same to read as follows:

--1. (Amended) A sampling frequency conversion apparatus for converting input data of a first sampling frequency into output data of a second sampling frequency, comprising:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read-out from said storage means to obtain the data of said second sampling frequency;

address difference [detector] detecting means for detecting an address difference between a [write] writable address and a [read] readable address in said storage means; and

address control means for performing an optimization operation optimizing the address difference detected by said address difference [detector] detecting means[;], wherein

said address control means adaptively sets a limitation on the [optimization] optimizing operation.

--2. (Amended) [A] The sampling frequency conversion apparatus according to claim 1, wherein

said address control means [so] works so as [will] not to execute the optimization operation when the address difference detected by said address difference [detector] detecting means [lies] falls within a predetermined range after [the] passage of

a predetermined period of time from [the start of supplying] a starting time when the input data is supplied.

--3. (Amended) [A] The sampling frequency conversion apparatus according to claim 1, wherein

said address control means [so] works so as [will] not to execute the optimization operation when the address difference detected by said address difference [detector] detecting means [lies] falls within a predetermined range after [the] passage of a predetermined period of time from [the switching on] a time when the power source circuit is switched on.

--4. (Amended) [A] The sampling frequency conversion apparatus according to claim 1, wherein

said predetermined period of time is longer than a time required for stabilizing [the] a ratio [of] between the first sampling frequency of the input data [to] and the second sampling frequency of the output data after [the] a start of supplying said input data.

--5. (Amended) [A] The sampling frequency conversion apparatus according to claim 1, wherein

said address control means [so] works so as [will] not to execute said optimization operation when the address difference detected by said address difference [detector] detecting means [lies] falls within a predetermined range after [the] passage of a predetermined period of time from [the

switching of] a time when the input data is initially supplied.

--6. (Amended) [A] The sampling frequency conversion apparatus according to claim 1, wherein

said address control means [works] performs a control operation to bring said address difference close to [an] a predetermined optimum value imposing no limitation when [the] a predetermined period of time has not been passed after [the] a start of supplying said input data or when the address difference detected by said address difference detector means [lies] falls outside [the] of a predetermined range.

--7. (Amended) [A] The sampling frequency conversion apparatus according to claim 6, wherein

said address control means executes the control operation [for] by bringing the address difference close to the predetermined optimum value by [so] judging that a moment at which the changing address difference value exceeds [an] the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.

--8. (Amended) A sampling frequency conversion apparatus having a plurality of sampling frequency conversion means for converting a first sampling frequency of input data into [any] a second sampling frequency to obtain output data, wherein

each of said plurality of sampling frequency conversion

means includes:

storage means into which said input data are continuously written and read-out;

interpolation processing means for interpolating the data read out from said storage means to obtain the data of said second sampling frequency;

address difference [detector] detecting means for detecting an address difference between a [write] writable address and a [read] readable address in said storage means;

and address control means for performing an optimization operation optimizing the address difference detected by said address difference [detector] detection means[; and], wherein[,]

said address control means [so] works so as [will] not to execute the optimization operation when the address difference detected by the address difference detector means in each of said plurality of sampling frequency conversion means [lies] falls within a predetermined range after [the] passage of a predetermined period of time from [the] a start of supplying said input data, thereby to eliminate a time difference [among] between the output data from said plurality of sampling frequency conversion means.

--9. (Amended) [A] The sampling frequency conversion apparatus according to claim 8, wherein

said predetermined period of time is longer than a time required for stabilizing [the] a ratio [of] between the first sampling frequency of the input data [to] and the second sampling

frequency of the output data after [the] a start of supplying the input data.

--10. (Amended) [A] The sampling frequency conversion apparatus according to claim 8, wherein

said address control means [works] performs a control operation to bring said address difference close to [an] a predetermined optimum value when [the] a predetermined period of time has not [been] passed after the start of supplying said input data or when the address difference detected by said address difference [detector] detecting means [lies] falls outside of the predetermined range.

--11. (Amended) [A] The sampling frequency conversion apparatus according to claim 10, wherein

said address control means executes the control operation [for] by bringing the address difference close to the predetermined optimum value by [so] judging that a moment at which the changing address difference value exceeds [an] the predetermined optimum value or becomes smaller than the predetermined optimum value, is the moment of an optimum address difference.